

Response
Serial No. 09/776,175
Page 7

REMARKS

In the Office Action, the Examiner noted that claims 1-26 are pending in the application and that claims 1-26 are rejected. The Examiner further noted that claims 21 and 22 are objected to but would be allowable if claim 21 was rewritten in independent form including all of the limitation of the base claim and any intervening claims. By this response claim 15 is amended to more clearly define the Applicant's invention and not in response to prior art. All other claims are unamended by this response.

In view of both the amendments presented above and the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in allowable form.

Rejections

A. 35 U.S.C. § 102(e)

The Examiner has rejected claims 1-4, 7, 8 and 20 under 35 U.S.C. § 102(e) as being anticipated by Treadaway et al. (U.S. Patent No. 6,665,285, hereinafter "Treadaway"). The rejection is respectfully traversed.

Regarding claim 1, the Examiner alleges that Treadaway teaches all of the aspects of the Applicant's invention. The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of **each and every element of the claimed invention**, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). The Applicant respectfully submits that Treadaway fails to disclose each and every element of the claimed invention, as arranged in at least the Applicant's claim 1, which specifically recites:

Response
Serial No. 09/776,175
Page 8

"A method of data communication, comprising:
transmitting a plurality of data frames temporally separated by
respective inter-packet gaps (IPGs), **each IPG having positioned within it
at least a synchronization pattern suitable for delineating a respective
data frame.**" (emphasis added).

In the Final Office Action, the Examiner alleges that features upon which the Applicant relies on in response to the First Office Action, specifically "the termination flag indicates the beginning of a control portion of a data stream where the data is divided into alternating control and data portions" is not recited in the rejected claims. The Applicant strongly disagrees.

The Applicant respectfully reminds the Examiner that inventors may act as their own lexicographers and use the specification to attribute specific meanings to terms in a patent claim. Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc., 262 Fed.3d 1258, 1268 (Fed. Cir. 2001). As such, claims must be read in view of the patent specification. *Id.* The Applicant further submits that for claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995). As such, the Applicant respectfully submits that features upon which the Applicant relies on in response to the First Office Action, specifically "the termination flag indicates the beginning of a control portion of a data stream where the data is divided into alternating control and data portions" is in fact recited in the rejected claims.

More specifically, with respect to the synchronization pattern, the Applicant specifically recites:

"The invention utilizes the IPG by embedding a long (e.g., 80-bit) termination flag (T-FLAG) within the IPG to operate as a synchronization pattern which will identify a control portion of the packetized data stream 200. As noted in FIG. 2, the 10 idle characters immediately following the EFD character in control portion C₂ are replaced by ten flag data characters

Response
Serial No. 09/776,175
Page 9

denoted as FD_1 through FD_{10} . In this manner, an 80-bit synchronization pattern is established. It is noted that the synchronization pattern may comprise more or less bytes, though it is important to insure that the number of bytes used for the synchronization pattern does not exceed the IPG implemented in a system processing the packetized data stream 200." (See Applicant's Specification, page 6, line 21 through page 7, line 1).

From at least the portion of the Applicant's Specification recited above, it is clearly evident that the Applicant in fact teaches and claims a termination flag in at least claim 1. More specifically, the Applicant teaches and claims the use of a synchronization pattern in an inter-packet gap used to delineate a respective data frame. The Applicant specifically teaches that in one embodiment of the invention, the synchronization pattern may be a termination flag. As such, it is very clear that the Applicant in fact teaches and claims using a termination flag as a synchronization pattern.

In addition, the Applicant absolutely also teaches and claims "the termination flag indicates the beginning of a control portion of a data stream where the data is divided into alternating control and data portions" as alleged by the Examiner as not being in the claims. More specifically, the Applicant in the Specification specifically recites:

"One embodiment of the invention operates within the physical coding sublayer (PCS) 175. The physical coding sublayer is responsible for frame delineation, frame formatting and line coding. The inventor protocol provides a mechanism for delineating frames or data payloads, formatting inter-frame control space according to a synchronization pattern and, optionally, one or more data patterns associated with a preceding data region.

The present invention is directed to simplifying the task of frame delineation. Frame delineation is a task of finding transition points between a data frame and a subsequent control frame, and between a control frame and a subsequent data frame. A transmitting PCS may associate each byte in an incoming data stream with either a data frame payload (datagram) or a "control frame" identifier. A start of frame delimiter (SFD), end of frame delimiter (EFD) and idle character are examples of the various control

Response
Serial No. 09/776,175
Page 10

characters employed for this task.” (See Applicant’s Specification, page 5, line 18, through page 6, line 2).

“The present invention provides a data structure, method, apparatus and protocol that utilizes the so-called inter-packet gap (IPG) to store a relatively long termination flag (T-FLAG) and a relatively short sequence identification nonce. The termination flag is used to indicate the beginning of a control portion of a data stream, where the data stream is divided into alternating control and data portions, each of the data portions comprising a packet or frame. Thus, the termination flag also indicates the end of a data frame.” (See Applicant’s Specification, Summary).

As such, because the Applicant in the Specification teaches that frame delineation includes at least of finding transition points between a data frame and a subsequent control frame, and between a control frame and a subsequent data frame, the Applicant respectfully submits that claim 1, in claiming that “a synchronization pattern suitable for delineating a respective data frame” in fact claims at least “the termination flag indicates the beginning of a control portion of a data stream where the data is divided into alternating control and data portions”.

Even further, in accordance with at least the Applicant’s claim 1 recited above, it is evident that the Applicant’s invention is directed at least in part to a method for data communication where respective synchronization patterns are positioned within inter-packet gaps between the data portions of communication signals for delineating a respective data frame. The presence and configuration of the inserted synchronization patterns are examined by a respective receiver to delineate respective data frames via the verification that an appropriate synchronization pattern has been received. In support of the claimed invention at least with respect to the Applicant’s claim 1, the Applicant in the Specification specifically recites:

“At step 520, termination flag data is inserted within the respective IPG. That is, at step 520A, a 9 to 12 byte (preferably) termination flag (T-FLAG) or synchronization pattern is appended to the data packet in a manner temporally occupying at least a portion of the 12 byte minimum inter-packet gap (IPG) previously discussed. The T-FLAG comprises a

Response
Serial No. 09/776,175
Page 11

unique bit pattern that will be detected by a receiver such that packet delineation may be determined." (See Applicant's Specification, page 11, lines 19-24).

"In one embodiment, a packet is accepted only when (1) an exact match of the start of packet (SOP) byte followed by payload (2) and by an exact match of the 10-byte T-FLAG and (3) the 2-byte length field is found. Either an early or later false match of T-FLAG and length field leads to false acceptance." (See Applicant's Specification, page 13, lines 21-24).

Again, it is very clear from at least the portion of the Applicant's Specification recited above, that the Applicant's invention of claim 1, is directed, at least in part, to a method of transmitting a synchronization pattern within data inter-packet gaps such that a receiver may determine packet delineation of respective data frames. Because the Applicant in the Specification teaches a specific meaning to the word "delineation", more specifically that a receiver looks for an exact match of a respective T-FLAG (synchronization pattern) for finding transition points between a data frame and a subsequent control frame, and between a control frame and a subsequent data frame, and because an inventor is his own lexicographer, the Applicant respectfully submits that the Applicant in at least claim 1, in fact specifically claims that respective synchronization patterns are transmitted in respective inter-packet gaps (IPGs), where the synchronization pattern is suitable for delineation of a respective data frame by a receiver in that the receiver looks for an exact match of a respective T-FLAG (synchronization pattern) for finding transition points between a data frame and a subsequent control frame, and between a control frame and a subsequent data frame.

In contrast to the Applicant's invention, there is absolutely no teaching, suggestion or disclosure in Treadaway for "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. More specifically, Treadaway fails to teach, suggest or disclose each and every element of the Applicant's claims arranged as in the

Response
Serial No. 09/776,175
Page 12

claims at least with respect to the Applicant's claim 1. Instead, Treadaway teaches a terminal for a wireless link in a metropolitan area network which includes a packet buffer for storing the data packets prior to storing the data packets in the rate buffer. A network switch can be a layer-two switch. The network switch can store the data packets in the packet buffer in response to a level of space available in the rate buffer, in response to rain fade in the wireless link, in response to interference in the wireless link, or in response to a detected bit error rate for communication via the wireless link. The terminal can include an extender device coupled to the broadcast device for receiving the data packets from the computer network and for providing the data packets to the broadcast device. (See Treadaway, Abstract). In support of its invention, Treadaway specifically recites:

"The rate control logic 250 detects each 100BASE-T Ethernet data packet received from the transceiver 212. In the preferred embodiment, the rate control block 250 then checks each such 100BASE-T Ethernet data packet for errors utilizing the frame check sequence (FCS) appended to each 100BASE-T Ethernet packet and strips each 100BASE-T Ethernet data packet of its preamble and start-of-frame delimiter (the frame-check sequence FCS for each 100BASE-T Ethernet packet is preferably retained). The rate control logic 250 also converts each Ethernet data packet from nibbles to bytes.

The rate control logic 250 calculates the length of each detected 100BASE-T Ethernet data packet. The rate control logic 250 also determines whether the packet is too long, too short (a runt packet) or is misaligned.

The rate control logic 250 then temporarily stores the packets in rate buffers 252. In the preferred embodiment, the bytes for each packet are clocked into the rate buffers 252 according a clock signal recovered from the data. The rate buffers 252 preferably include two first-in, first-out (FIFO) buffers having 16 K entries, one for packets being transmitted and one for packets being received. The FIFO buffers each preferably provides sufficient storage for each entry so that additional information can be stored in the rate buffers 252 along with the byte of data. Such additional information preferably includes the data valid bit for each nibble and an indication of whether the nibble is payload data or overhead for the 100BASE-T Ethernet packets. For example, the overhead can include inter-packet gaps codes (e.g. one byte/octet of all zeros with associated data

Response
Serial No. 09/776,175
Page 13

valid bits de-asserted), and start-of-packet codes. Assuming inter-packet gap codes are stored, preferably only one inter-packet gap code, representative of the minimum required inter-packet gap (e.g. of 0.96 μ s), is stored in the rate buffers 252.

At optional step 530, a first type of nonce is generated and utilized. Specifically, at step 532, the number of double words in the received packet is calculated and, at step 534, the double word count is inserted within the respective IPG." (See Treadaway, col. 11, lines 11-51).

As evident from at least the portion of Treadaway recited above, it is clear that the invention of Treadaway is directed to an Ethernet switch in a terminal including a MAC where the MAC includes a rate control logic device. The rate control logic device of Treadaway detects each data packet received from a transceiver and calculates the length of each data packet. The rate control logic device then temporarily stores the packets in rate buffers. Along with the data packet, additional information regarding the data packet is stored. For example, overhead can include inter-packet gaps codes. The inter-packet gap codes taught in Treadaway represent the minimum required inter-packet gaps for the transmission of the data packets. Treadaway specifically teaches that during periods when a complete packet is not available from the rate buffers, then an inter-packet gap code is substituted by the packet synch/de-synch block. (See Treadaway, col. 10, line 58 to col. 11, line 67). There is however, absolutely no teaching, suggestion or disclosure in Treadaway for "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), **each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame**" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 1. In fact, Treadaway is completely silent about inter-packet gaps between transmitted data signals.

More specifically, the Applicant specifically teaches that an "inter-packet gap comprises a pause between back-to-back transmissions." (See Applicant's Specification, page 4, lines 17-18). Treadaway makes absolutely no reference at all to inter-packet gaps between back-to-back data transmissions. Even further,

Response
Serial No. 09/776,175
Page 14

Treadaway does not teach or suggest the transmission of a synchronization pattern in inter-packet gaps of data packets such that the unique bit pattern will be detected by a receiver such that packet delineation may be determined as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

Instead in Treadaway, a data packet is stored in a rate buffer, and along with the data packet, information regarding a minimum required inter-packet gap for the data packet may also be stored in a packet header. In fact, in the Final Office Action, the Examiner stated that Treadaway teaches a reformed data frame in figure 5, element 300, which is loaded to rate buffers depicted in figure 4, element 252. By the Examiner's own admission, the teachings of Treadaway teach away from the invention of the Applicant. Specifically, and as conceded by the Examiner, Treadaway teaches reforming a data frame to include information such as packet length and inter-packet gap codes to separate each data packet. (See Treadaway, col. 16, lines 45-47). This is in direct contrast to the invention of the Applicant which teaches and claims "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame", wherein there is no need to reform a data frame as taught by Treadaway and as conceded by the Examiner. In fact, the Applicant specifically recites that the invention of the Applicant has distinct advantages over prior art teachings such as Treadaway. That is, in the Specification, the Applicant specifically recites:

"The described simple data link (SDL) protocol provides for the framing of asynchronous protocol data units (PDUs) using a length indicator and pointer scheme whereby a pointer in the header of one packet or data frame is used to identify the start of a next packet or data frame. The SDL utilizes a length indicator field and a header cyclic redundancy check (CRC) to delineate frames. Unfortunately, in the case where packet length information is not available, an entire packet must be stored, thereby increasing latency. This may not be acceptable in some applications, such as "cut-through" packet switching." (See Applicant's Background, page 2, lines 16-23).

Response
Serial No. 09/776,175
Page 15

"Since the IPG is already required, the frame delineation scheme adds no additional overhead. It will be shown that such a scheme is robust in the presence of both burst and random errors." (See Applicant's Summary, page 3, lines 18-20).

As clearly evident from at least the portions of the Applicant's disclosure presented above, the Applicant's invention has a clear advantage over the invention of Treadaway as there is no need in the Applicant's invention to reform a data frame as taught in Treadaway and as conceded by the Examiner. For at least the reasons stated above, the Applicant respectfully submits that there is absolutely no teaching, suggestion, disclosure or even mention of "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs)" wherein "each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. In fact there is absolutely no teaching, suggestion or disclosure in Treadaway of inserting absolutely anything into inter-packets gaps between transmitted data frames. The only mention of inter-packet gap in Treadaway is for the teaching of an inter-packet gap code that is inserted in the header of a reformed data frame to indicate a minimum packet gap required between data frames.

Even further the Applicant submits that there is absolutely no teaching, suggestion or disclosure in Treadaway for a synchronization pattern as taught in the Applicant's specification and claimed by at least the Applicant's claim 1. As depicted above, the Applicant teaches a specific and unique synchronization pattern that is positioned in a respective inter-packet gap which is subsequently identified and examined by a receiver for the delineation of a respective data frame. Instead in contrast to the invention of the Applicant, Treadaway specifically recites:

"Upon retrieving each packet from the rate buffers, the packet synch/de-synch block 256 adds a synch pattern in field 302 and a length

Response
Serial No. 09/776,175
Page 16

value in field 304 to the packet. The length value is retrieved from the length and status buffer 254.

The packet synch/de-synch block 256 retrieves the stored 100BASE-T Ethernet data packets from the rate buffers 252 at an appropriate rate which depends, in part, upon the data transmission rate utilized for sending data over the wireless link 102. In the preferred embodiment, removal of data from the rate buffers 252 for an Ethernet packet is not initiated until the packet has been completely stored." (See Treadaway, col. 11, lines 58-64).

In the preferred embodiment, finite state machines control the synch/de-synch block 256 so as to enable the retrieval of 100BASE-T Ethernet packets from the rate buffers 252 along with the length and status of each, at a appropriate frequency for forming radio frames 350 (FIG. 6). (See Treadaway, col. 12, lines 8-19).

As evident from at least the portions of Treadaway presented above, Treadaway teaches adding a synch pattern in a reformed data frame for enabling the retrieval of the stored 100BASE-T Ethernet data packets from the rate buffers 252 at an appropriate rate which depends, in part, upon the data transmission rate utilized for sending data over the wireless link. However there is absolutely no teaching, suggestion or disclosure in Treadaway for a "synchronization pattern suitable for delineating a respective data frame" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

For at least the reasons stated above, the Applicant strongly and respectfully submits that Treadaway absolutely fails to teach, suggest or disclose each and every element of the Applicant's claimed invention arranged as in the Applicant's claims as required for anticipation of the Applicant's claims.

Therefore, the Applicant submits that claim 1 is not anticipated by the teachings of Treadaway and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claims 10, 15 and 20 recite similar relevant features as recited in claim 1. As such, and for at least the reasons stated herein, the Applicant submits that claims 10, 15 and 20 are also not anticipated by the teachings of Treadaway and, as such, also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

Response
Serial No. 09/776,175
Page 17

Furthermore, dependent claims 2-9, 11-14, 16-19, and 21-26 depend either directly or indirectly from independent claims 1, 10, 15 and 20 and recite additional limitations therefor. As such, and for at least the reasons set forth herein, the Applicant submits that none of these claims are anticipated by the teachings of Treadaway. Therefore, the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

B. 35 U.S.C. § 103(a)

The Examiner has rejected claims 5, 6, 11, 12, 14-19 and 23 under 35 U.S.C. § 103(a) as being unpatentable over Treadaway in view of Rouse (U.S. Patent No. 5,260,933). The rejection is respectfully traversed.

Claims 5 and 23

Regarding claims 5 and 23, the Examiner alleges that Treadaway teaches all of the limitations of the Applicant's invention except that Treadaway fails to teach "CRC" for detecting errors data element generated and positioned within the data frame. As such, the Examiner cites Rouse for teaching "CRC" for detecting errors data element generated and positioned within the data frame. The Applicant respectfully disagrees.

The Examiner applied Treadaway for the rejection of claims 5 and 23 as applied above for the Examiner's rejection of claims 1 and 20. For at least the reasons recited above, the Applicant respectfully submits that the teachings of Treadaway, alone do not teach, suggest or disclose at least the Applicant's claims 1 and 20. More specifically, Treadaway does not teach, suggest or disclose "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught by the

Response
Serial No. 09/776,175
Page 18

Applicant's Specification and claimed in at least the Applicant's claim 1 and claim 20. That is, Treadaway does not teach or suggest the transmission of a synchronization pattern in inter-packet gaps of data packets such that the unique bit pattern will be detected by a receiver such that packet delineation may be determined. As such, and for at least the reason that Treadaway does not teach, suggest or disclose the Applicant's claims 1 and 20, the Applicant further submits that Treadaway also does not teach, suggest or disclose the Applicant's claims 5 and 23, which depend from claims 1 and 20 and recite additional limitations therefor.

In addition, the Applicant respectfully submits that the teachings of Rouse alone, also do not teach, suggest or disclose the invention of the Applicant, at least with respect to independent claims 1 and 20 and dependent claims 5 and 23. More specifically, Rouse teaches a system and method for controlling the transmission of frames or packets of data in a serial network which allows out-of-order delivery. In Rouse, the data frames transmitted by an initiator node to the recipient node include frame serial number or sequence count information. However, there is absolutely no teaching, suggestion or disclosure in Rouse for "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 1 and claim 20. That is, Rouse does not teach or suggest the transmission of a synchronization pattern in inter-packet gaps of data packets such that the unique bit pattern will be detected by a receiver such that packet delineation may be determined. As such, and for at least the reason that Rouse does not teach, suggest or disclose the Applicant's claims 1 and 20, the Applicant further submits that Rouse also does not teach, suggest or disclose the Applicant's claims 5 and 23, which depend from claims 1 and 20 and recite additional limitations therefor.

Furthermore, the Applicant submits that there is absolutely no motivation or suggestion in either reference for the combination of Treadaway and Rouse to

Response
Serial No. 09/776,175
Page 19

attempt to teach the invention of the Applicant. More specifically, there is obviously no motivation or suggestion in Treadaway for the combination of the references. Likewise, Rouse does not expressly or impliedly motivate or suggest such a combination.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). ***Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention*** Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983). (emphasis added)

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Applicant further submits that even if there was a motivation or suggestion to combine (which the Applicant maintains that there is not), the teachings of Treadawya and Rouse, in any allowable combination, fail to teach, suggest or make obvious the Applicant's invention, at least with regard to independent claims 1 and 20 and in addition, with respect to claims 5 and 23, which depend from claims 1 and 20 and recited additional limitations therefor. More specifically, the teachings of Treadaway and Rouse fail to teach, suggest or make obvious "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught

Response
Serial No. 09/776,175
Page 20

by the Applicant's Specification and claimed in at least the Applicant's claim 1 and claim 20. That is, any allowable combination of Treadaway and Rouse does not teach or suggest the transmission of a synchronization pattern in inter-packet gaps of data packets such that the unique bit pattern will be detected by a receiver such that packet delineation may be determined.

As such and for at least the reasons described above, the Applicant respectfully submits that neither the Ethernet switch taught in Treadaway nor the acknowledgment protocol taught in Rouse, alone or in any allowable combination, renders obvious the "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 1 and claim 20. As such and for at least the reason that Treadaway and Rouse, alone or in any allowable combination, fail to teach or suggest the invention of the Applicant with regard to claims 1 and 20, the Applicant further submits that the teachings of Treadaway and Rouse, alone or in any allowable combination, also fail to teach or suggest the invention of the Applicant with regard to claims 5 and 23, which depend from claims 1 and 20.

Therefore, the Applicant submits that claims 5 and 23 as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Likewise dependent claims 6, 11-12, 14, and 16-19 depend either directly or indirectly from independent claims 1, 10, and 15. As stated above and for at least the reasons stated above with respect to claim 1, the Applicant respectfully submits that Treadaway fails to anticipate the Applicant's claims 10 and 15, which recite similar relevant features as the Applicant's claim 1. In addition and for at least the reasons stated above with respect to claim 1, the Applicant respectfully submits that the teachings of Treadaway and Rouse, alone or in any allowable combination also fail to make obvious the Applicant's claims 10 and 15, which recite similar relevant features as the Applicant's claim 1. As such, and for at least the reasons stated above, the Applicant submits that dependent claims 6, 11-12,

Response
Serial No. 09/776,175
Page 21

14, and 16-19, which depend from independent claims 1, 10 and 15 are also not obvious with respect to the teachings of Treadaway and Rouse, alone or in any allowable combination. Therefore the Applicant submits that dependent claims 6, 11-12, 14, and 16-19 also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

C. 35 U.S.C. § 103(a)

The Examiner has rejected claims 9, 10, 13 and 24-26 under 35 U.S.C. § 103(a) as being unpatentable over Treadaway. The rejection is respectfully traversed.

Claims 9 and 24-26

Regarding claims 9 and 24-26, the Examiner alleges that Treadaway teaches all of the limitations of the Applicant's invention except that Treadaway fails to teach a pointer data element for indicating the position of next data element. However, the Examiner alleges that it would have been obvious to one skilled in the art at the time the invention was made that a pointer is required in the data structure to locate and identify a location in internal storage. The Applicant respectfully disagrees.

The Examiner applied Treadaway for the rejection of claims 9 and 24-26 as applied above for the Examiner's rejection of claims 1 and 20. For at least the reasons recited above, the Applicant respectfully submits that the teachings of Treadaway, alone do not teach, suggest or disclose at least the Applicant's claims 1 and 20. More specifically, Treadaway does not teach, suggest or disclose "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization

Response
Serial No. 09/776,175
Page 22

pattern suitable for delineating a respective data frame" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 1 or "determining data frame delineation points within a received data stream by detecting the presence of a synchronization pattern within said data stream, said synchronization pattern being positioned within inter-packet gaps" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 20. That is, Treadaway does not teach or suggest the transmission of a synchronization pattern in inter-packet gaps of data packets such that the unique bit pattern will be detected by a receiver such that packet delineation may be determined. As such, and for at least the reason that Treadaway does not teach, suggest or disclose the Applicant's claims 1 and 20, the Applicant further submits that Treadaway also does not teach, suggest or disclose the Applicant's claims 9 and 24-26, which depend from claims 1 and 20 and recite additional limitations therefor.

As such and for at least the reasons described above, the Applicant respectfully submits that the Ethernet switch taught in Treadaway does not render obvious the "transmitting a plurality of data frames temporally separated by respective inter-packet gaps (IPGs), each IPG having positioned within it at least a synchronization pattern suitable for delineating a respective data frame" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 1 and "determining data frame delineation points within a received data stream by detecting the presence of a synchronization pattern within said data stream, said synchronization pattern being positioned within inter-packet gaps" as taught by the Applicant's Specification and claimed in at least the Applicant's claim 20. As such and for at least the reason that Treadaway fails to teach or suggest the invention of the Applicant at least with regard to claims 1 and 20, the Applicant further submits that the teachings of Treadaway also fail to teach or suggest the invention of the Applicant with regard to claims 9 and 24-26, which depend from claims 1 and 20.

Response
Serial No. 09/776,175
Page 23

Therefore, the Applicant submits that claims 9 and 24-26 as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Likewise, independent claim 10 recites similar relevant features as recited in claim 1. As such, and for at least the reasons stated herein, the Applicant submits that claim 10 is also not rendered obvious by the teachings of Treadaway and, as such, also fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claim 13 depends directly from independent claim 10 and recites additional limitations therefor. As such, and for at least the reasons stated herein, the Applicant submits that dependent claim 13 is also not obvious with respect to the teachings of Treadaway. Therefore the Applicant submits that dependent claims 13 also fully s the requirements of 35 U.S.C. § 103 and is patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

Applicant's Note

The Applicant would like to thank the Examiner for the indication of allowable subject matter and agree with the Examiner that claims 21 and 22 would be allowable if claim 21 was rewritten in Independent form including all of the limitation of the base claim and any intervening claims, however at this time the Applicant submits that all of the Applicant's claims are patentable over the prior art presently cited against the Applicant's invention.

Conclusion


Thus the Applicant submits that none of the claims, presently in the application, are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both

Response
Serial No. 09/776,175
Page 24

reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 530-9404 x 1131 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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Dated: 6/17/04

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